JCS BN-1 4-BIT LINEAR PCM SYNTHESIZER

CIRCUIT DESCRIPTION

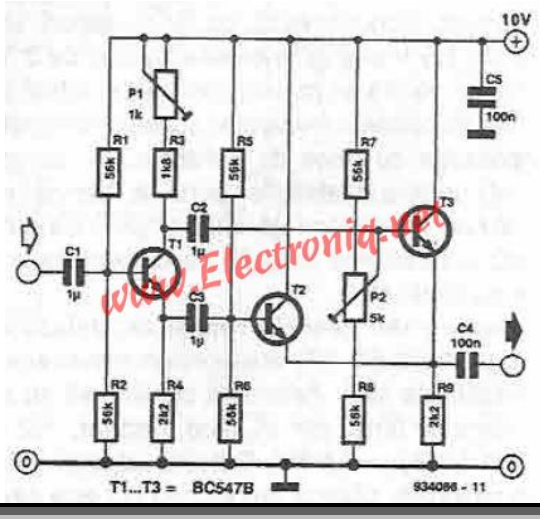
These descriptions assume some familiarity with electronics, especially with respect to component types (resistors, capacitors, etc.), measuring voltages, ICs (TTL, op-amps), and digital logic (AND, OR, etc.). All listed voltages are measured with respect to ground. It may be useful to know the Russian alphabet.

Also, note that the TTL chips, which are mostly in the K155… / 74… series, could possibly be replaced with chips in other series with no ill effect. For example, the K155TM7 / 7475 could be replaced with a K555TM7 / 74LS75. The listed series are simply the types that were used in the JCS-built unit.

SCHEMATIC 1
CLOCK-RELATED & PROGRAM SELECTION CIRCUITS

FREQUENCY DOUBLER – Based on the design shown below, originally found at Electroniq.net, this is built around the three NPN transistors Q1, Q2, and Q3. Using a sinewave input, trimmers R8 and R9 are adjusted so that the output is as sinusoidal as possible. The 9V supply is used instead of the 5V in order to have the highest possible amplitude at the output, which is still typically considerably lower than the amplitude of the input signal. The following description is directly quoted from Electroniq.net:

"When the input signal is> the 1V T2 and T3 works as rectifier, meaning it fundamental frequency of the input signal is automatically doubled. The input signals <1V two T1 signals in antiphase products of the input signal is brought in emitters of T2 and T3 and summed. This means that virtually disappears fundamental frequency, so that, due to nonlinearities, remain only harmonics: first harmonic is now fundamental frequency output signal. Thus resulting in a considerable attenuation of the input signal: a signal input of 25 mV remain only 6 mV output. Assuming a sinusoidal input signal, the fundamental frequency rejection is optimized by P1. T3's operating point will be adjusted by the P2 for an output signal as close to a sinusoidal. Input frequency range extends from 80 Hz to above the 100 kHz frequency."



INTERNAL CLOCK OSCILLATOR & COMPARATORS – Three of the four comparators are used within IC1 (LM339): two for providing TTL-compatible clock signals from the analog sources (external input and frequency doubler output), and one acting as an oscillator within the approximate range of 1200-7200 Hz.

The oscillator is a simple design that is intended mainly for testing. The non-inverting (+) input of the comparator is held at around 2.5V by the voltage divider formed by R24 and R25. Assuming the output starts high (with the voltage at the inverting input below the non-inverting), the capacitor C6 charges through resistor R26 and potentiometer R69 until the voltage at the inverting (-) input exceeds that at the non-inverting, at which point the comparator output goes low, and the capacitor C6 drains through the resistors until the voltage is below the non-inverting input, at which point the output goes high. Of course, this process repeats, and thus oscillation occurs. R22 limits the gain of the comparator, and therefore limits the rate at which the output changes from high to low (i.e. provides hysteresis). R23, as well as R72 and R73 on the other comparators, are pull-up resistors that allow the open-collector outputs to go high. If desired, R26 and C6 in particular can be changed to provide different frequency ranges.

Comparator circuits for generating TTL clocks from the doubled and non-doubled analog signals are identical. R16 and R17 form a voltage divider to hold the inverting inputs of both comparators at around 2.5V, and with C12 reducing high frequency noise on this node. Each input signal is fed through a decoupling capacitor and 10 kΩ resistor to the non-inverting inputs, where there are also voltage dividers to put a DC bias on the signals of about 2.5V. R12 and R18 provide hysteresis.

CLOCK SELECT SWITCH & PROGRAM ENABLE – A 3-position toggle switch is used to select between the external, frequency doubled external, and internal clock sources. The signal selected by the switch is passed to one of the two input pins of the first NAND gate of IC4 (7400), which contains four gates in total, one unused. The other pin of the first gate is connected to the !PROG_EN (program enable) line, which is active low, and which is normally high (due to pull-up resistor R38) and can be brought low by a toggle switch. So, the selected clock signal is only passed through the gate (inverted, of course) when PROG_EN is high, since the clock should only be "activated" when not in programming mode. Note that the program enable line is used by other parts of the circuit in schematics 2 and 3.

SCHEMATIC 2
PROGRAM COUNTER, RESET LOGIC, OFFSET ADDERS, ADDRESS MULTIPLEXERS

PROGRAM COUNTER – Based around IC6 and IC7, which are both 7493 4-bit binary counters. The clock inputs, CKA and CKB, are triggered on the falling edge. From the output of the first gate of IC4, the CLOCK signal is fed to the CKA input of the upper counter. For both, in order for the full counting range (0000 to 1111) to be used, the least significant output bit, QA, is connected to the CKB clock input. All reset (R0) inputs of both counters are connected to the reset signal provided by the reset logic (see below).

RESET LOGIC – This is composed of three gates, a switch, and a button. First, all four data lines (D1 to D4) are fed to the first gate of IC8 (7425), which is a dual 4-input NOR. When all four data lines are low (data is 0000), the output of this gate goes high, and is connected to one input of the second gate of IC8 through a switch S3, the "Loop Enable" switch. If the switch is closed, then when the number 0000 appears on the data bus, the output of the second gate of IC8 will go low, and will be inverted by the fourth gate of IC4 (2-input NAND), which is connected to the reset lines of the two counters IC6 and IC7, thus resetting the counters. The momentary (normally open) "Count Reset" button S4 performs the same function, being connected to another one of the inputs to the second gate of IC8.

ADDRESS OFFSET ADDERS – Composed of IC11 and IC12, which are two types of 4-bit adders: a 74LS283 and К155ИМ3 / 7483. In fact, both perform the same function, although they have different pinouts. Thus, the circuit could be easily modified to have both of one type or the other by simply altering one chip's pinout.

Each program counter chip is paired to an adder, with its outputs fed into the adder's "A" inputs (A1 to A4). To the "B" set of inputs, the address entry switches are connected. This allows the starting address of the sample playback to be set with the address switches while in running mode. The upper chip's carry input (C0) is brought low, and the carry output (C4) is fed into the carry input of the lower chip.

ADDRESS MULTIPLEXERS – These are used to select between the outputs of the offset adders and the address entry switches, and based around IC9 and IC10, both 74LS157. Switching is done based on the program enable line; when it is low/enabled, the address entry switches are passed to the mux. outputs, and when high, the offset adder outputs are passed to the mux. outputs. These output lines are named A1 to A8, and these are the main address outputs that are fed to the memory chips.

SCHEMATIC 3
MEMORY, DATA INPUT, DAC, & AUDIO OUTPUT

RAM & ROM – SRAM is comprised of a single 2112 chip, IC2, and ROM is comprised of a single К155РЕ2X, IC15, where X = 1, 2, 3, or 4. Both chips are 256 x 4, so they take an 8-bit address input and give a 4-bit number at the outputs (which also function as data inputs, in the case of the RAM). The Soviet ROMs are clones of 74187 PROM chips, although they are factory-programmed with some sort of character conversion data. For example, the К155РЕ21 apparently converts some form of binary-encoded characters to some form of encoded Russian characters. (Let me know if you figure out exactly what these chips are supposed to do – see the "contact" page at http://jcs.deadmau6.com)

A switch, S10, is used to enable either ROM or RAM, although a NAND gate, the third gate of IC4, makes it impossible to select the ROM during programming mode. Thus, if the switch is in the "ROM" position and programming mode is enabled, neither chip will be enabled.

Button S12, a momentary switch normally open, allows the data present on the data entry switches to be written to RAM. Note that programming mode does not have to be enabled for this to function, but there is really no reason to use it outside of programming mode unless the clock speed is extremely low. Aside from bringing the write enable line low on the SRAM chip, it also has a function in the next section.

DATA INPUT BUFFER – Composed of IC16, which is a К155ЛН6 / 74366 hex inverting buffer with tri-state outputs. The inverting nature of the buffers is not important, however, the tri-state outputs are. In this arrangement, outputs of this chip are normally in "High-Z" mode, essentially "shut off". The outputs are only enabled when the write button is pressed, and so the data from the data entry switches goes onto the data bus right when the chip's write enable line is enabled.

OUTPUT LATCH & DAC – The output latch is composed of IC3, which is a К155ТМ7 / 7475 4-bit bistable latch. In early revisions, this latch was actually clocked, but in this final design, it simply acts as an inverting buffer for the DAC, which itself is composed of resistors R28 to R36. These are weighted so that the most significant bit (representing a difference of 8) has a resistance on the output 1/8 of that of the least significant (representing a difference of 1), so in this case, 5 kΩ on the MSB and 40 kΩ on the LSB. The reason the inverted outputs are used instead of the non-inverted outputs is due to the behavior of the next section: the output op-amp is set up in an inverting configuration. So, since the signal essentially gets inverted twice, the result is a non-inverted signal at the output.

OUTPUT BUFFER OP-AMP – In order to drive a significant load at the output (such as an amp, mixer, etc.), the output impedance needs to be relatively low. This is why there is an output buffer rather than simply connecting the node of the resistors after the DAC to the output. It consists of IC5, a КР140УД1Б, which is the only chip in the unit for which there is no pin-compatible "Western" equivalent, although it is apparently based on the μA702 (the first op-amp ever commercially available). It would not be difficult to modify the circuit to use a different op-amp, of course.

The most important thing to note in this circuit is the capacitor C30, which is used to suppress ultrasonic oscillation, which this circuit is very prone to if this capacitor is not installed or not sufficiently large.

SCHEMATIC 4
LED DISPLAYS, POWER CIRCUITRY, DECOUPLING CAPS

ADDRESS BUS DISPLAY – Based on IC13, a К555АП3 / 74LS240 8-bit inverting buffer. It is really quite simple, with LED5 to LED12 providing indication for each bit in the address bus.

DATA BUS DISPLAY – Very similar to the address bus display, except using IC14, a К155ЛН1 / 7404 hex inverter, with two gates unused.

POWER CIRCUITRY – Jack J1 accepts a 9-12V DC power source, tip positive. D1 protects against reverse polarity of the power supply. IC17, a LM323K provides the regulated 5 V supply essential to powering the TTL chips. Both this regulated "+5V" supply and the "+9V" supply are passed to the circuit, though the "+9V" supply will have a reduction compared to the input of about 0.7V due to the polarity protection diode. Also, IC17 should have a heatsink.

DECOUPLING CAPACITORS – One for each chip (excluding IC17).